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Subclass
Class
ISSUE CLASSIFICATION

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PATENT NUMBER

U.S. UTILITY Patent Application

	O.I.P.E. Q.A. 
SCANNED	PATENT DATE

APPLICATION NO. 09/942328	CONT/PRIOR	CLASS <u>365</u> <u>711</u>	SUBCLASS <u>141</u>	ART UNIT <u>2918</u> <u>2186</u>	EXAMINER <u>M. Kim</u> <u>H. Kim</u>
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APPLICANTS

Padmanabha Venkitakrishnan
Shankar Venkataraman
Stuart Siu

TITLE

Streamlined cache coherency protocol system and method for a multiple processor single chip device

ISSUING CLASSIFICATION

Continued on Issue Slip Inside File Jacket

TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.				NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____				ISSUE FEE	
	(Assistant Examiner)	(Date)		Amount Due	Date Paid
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